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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/854,865	05/14/2001	Michael Philip McIntosh	TUC920010006US1	9915

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EXAMINER	
KNOLL, CLIFFORD H	

ART UNIT	PAPER NUMBER
2112	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/854,865	MCINTOSH ET AL.	
	Examiner	Art Unit	
	Clifford H Knoll	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3, 10, and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 3 and 10, the recitation of a "wherein said ... frame ... generating" does not make sense; perhaps "generates" is intended; nor is it clear the relationship of the recited generated pulse to previously recited pulse generation.

In claim 14, the frame pulse is unclear because its relationship to the previously recited claim pulse has not been clearly established.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-36 are rejected under 35 U.S.C. 102(e) as being anticipated by Beyers (US 6072804).

Regarding claim 1, Beyers discloses a plurality of individual frames connected in series, a multi-channel bus coupled to each frame (e.g., col. 2, line 66 – col. 3, line 12), a power bus return bus carrying information indicative of the last frame (e.g., col. 3, lines 10-12), where one of the frames is a first frame (e.g., col. 4, lines 17-20) a signal indicative of power being supplied to it and generating a delayed signal each subsequent frame receiving said delayed signal and generating a further delayed signal and each frame generating a pulse on said frame bus (e.g., col. 4, lines 15-17), one of said frames being defined as said last frame and receiving said delayed signal and generating a signal to activate said power return bus (e.g., col. 4, lines 26-31) and wherein the total count counter being incremented by each said pulse until said power return is activated (e.g., col. 8, lines 5-9).

Regarding claim 2, Beyers also discloses where the total count counter represents the total number connected together (e.g., col. 19, lines 22-24).

Regarding claim 3, Beyers also discloses wherein at least one said frame generates a frame pulse (e.g., col. 4, lines 15-17).

Regarding claim 4, Beyers also discloses an ID counter being incremented by each said pulse (e.g., col. 8, line 6).

Regarding claim 5, Beyers also discloses the ID counter represents the individual ID (e.g., col. 8, line 6).

Regarding claim 6, Beyers also discloses the delayed signal has an approximately constant predetermined value (e.g., col. 6, lines 28-30).

Regarding claim 7, the delayed signal has a variable delay value (e.g., col. 6, lines 60-61).

Regarding claim 8, Beyers discloses a plurality of individual frames connected in series, a multi-channel bus coupled to each frame (e.g., col. 2, line 66 – col. 3, line 12), a power bus return bus carrying information indicative of the last frame (e.g., col. 3, lines 10-12), where one of the frames is a first frame (e.g., col. 4, lines 17-20) a signal indicative of power being supplied to it and generating a delayed signal each subsequent frame receiving said delayed signal and generating a further delayed signal and each frame generating a pulse on said frame bus (e.g., col. 4, lines 15-17), one of said frames being defined as said last frame and receiving said delayed signal and generating a signal to activate said power return bus (e.g., col. 4, lines 26-31) and wherein the total count counter being incremented by each said pulse until said power return is activated (e.g., col. 8, lines 5-9).

Regarding claim 9, Beyers also discloses where the total count counter represents the total number connected together (e.g., col. 19, lines 22-24).

Regarding claim 10, Beyers also discloses wherein at least one said frame generates a frame pulse (e.g., col. 4, lines 15-17).

Regarding claim 11, Beyers also discloses an ID counter being incremented by each said pulse (e.g., col. 8, line 6).

Regarding claim 12, Beyers also discloses the ID counter represents the individual ID (e.g., col. 8, line 6).

Regarding claim 13, Beyers discloses coupling a plurality of individual frames connected in series, a multi-channel bus coupled to each frame (e.g., col. 2, line 66 – col. 3, line 12), designating a last frame (e.g., col. 3, lines 10-12), designating one of the frames as a first frame (e.g., col. 4, lines 17-20) receiving a signal indicative of power being supplied to it and generating a delayed signal each subsequent frame receiving said delayed signal and generating a further delayed signal and each frame generating a pulse on said frame bus (e.g., col. 4, lines 15-17), generating a signal to activate said power return bus (e.g., col. 4, lines 26-31) and incrementing a register by each said pulse until said power return is activated (e.g., col. 8, lines 5-9).

Regarding claim 14, Beyers also discloses generating a frame pulse and incrementing a register (e.g., col. 19, lines 22-24).

Regarding claim 15, Beyers also discloses the ID counter represents the individual ID (e.g., col. 8, line 6).

Regarding claim 16, Beyers also discloses where the total count counter represents the total number connected together (e.g., col. 19, lines 22-24).

Regarding claim 17, Beyers discloses a plurality of individual frames connected in series, a multi-channel bus coupled to each frame (e.g., col. 2, line 66 – col. 3, line 12), a power bus return bus carrying information indicative of the last frame (e.g., col. 3, lines 10-12), where one of the frames is a first frame (e.g., col. 4, lines 17-20) a signal indicative of power being supplied to it and generating a delayed signal each

subsequent frame receiving said delayed signal and generating a further delayed signal and each frame generating a pulse on said frame bus (e.g., col. 4, lines 15-17), one of said frames being defined as said last frame and receiving said delayed signal and generating a signal to activate said power return bus (e.g., col. 4, lines 26-31) and wherein the individual ID counter being incremented by each said pulse until said power return is activated (e.g., col. 8, lines 5-9).

Regarding claim 18, Beyers also discloses where the total count counter represents the total number connected together (e.g., col. 19, lines 22-24).

Regarding claim 19, Beyers also discloses a power return bus carrying information indicative of the last frame and receiving said delayed signal and generating a signal to activate said power return bus (e.g., col. 4, lines 26-31).

Regarding claim 20, Beyers also discloses the total count counter being incremented by each said pulse until said power return is activated (e.g., col. 8, lines 5-9).

Regarding claim 21, Beyers also discloses where the total count counter represents the total number connected together (e.g., col. 19, lines 22-24).

Regarding claim 22, Beyers discloses a plurality of individual frames connected in series, a multi-channel bus coupled to each frame (e.g., col. 2, line 66 – col. 3, line 12), a power bus return bus carrying information indicative of the last frame (e.g., col. 3, lines 10-12), where one of the frames is a first frame (e.g., col. 4, lines 17-20) a signal indicative of power being supplied to it and generating a delayed signal each subsequent frame receiving said delayed signal and generating a further delayed signal

and each frame generating a pulse on said frame bus (e.g., col. 4, lines 15-17), one of said frames being defined as said last frame and receiving said delayed signal and generating a signal to activate said power return bus (e.g., col. 4, lines 26-31) and wherein the individual ID counter being incremented by each said pulse until said power return is activated (e.g., col. 8, lines 5-9).

Regarding claim 23, Beyers also discloses the ID counter represents the individual ID (e.g., col. 8, line 6).

Regarding claim 24, Beyers also discloses a power return bus carrying information indicative of the last frame and receiving said delayed signal and generating a signal to activate said power return bus (e.g., col. 4, lines 26-31).

Regarding claim 25, Beyers also discloses the total count counter being incremented by each said pulse until said power return is activated (e.g., col. 8, lines 5-9).

Regarding claim 26, Beyers also discloses where the total count counter represents the total number connected together (e.g., col. 19, lines 22-24).

Regarding claim 27, Beyers discloses coupling a plurality of individual frames connected in series, a multi-channel bus coupled to each frame (e.g., col. 2, line 66 – col. 3, line 12), designating a last frame (e.g., col. 3, lines 10-12), designating one of the frames as a first frame (e.g., col. 4, lines 17-20) receiving a signal indicative of power being supplied to it and generating a delayed signal each subsequent frame receiving said delayed signal and generating a further delayed signal and each frame generating a pulse on said frame bus (e.g., col. 4, lines 15-17), generating a signal to activate said

power return bus (e.g., col. 4, lines 26-31) and incrementing a register by each said pulse until said power return is activated (e.g., col. 8, lines 5-9).

Regarding claim 28, Beyers also discloses generating a frame pulse and incrementing a register (e.g., col. 19, lines 22-24).

Regarding claim 29, Beyers also discloses the ID counter represents the individual ID (e.g., col. 8, line 6).

Regarding claim 30, Beyers also discloses where the total count counter represents the total number connected together (e.g., col. 19, lines 22-24).

Regarding claim 31, Beyers discloses a plurality of individual frames connected in series, a multi-channel bus coupled to each frame (e.g., col. 2, line 66 – col. 3, line 12), a power bus return bus carrying information indicative of the last frame (e.g., col. 3, lines 10-12), where one of the frames is a first frame (e.g., col. 4, lines 17-20) a signal indicative of power being supplied to it and generating a delayed signal each subsequent frame receiving said delayed signal and generating a further delayed signal and each frame generating a pulse on said frame bus (e.g., col. 4, lines 15-17), one of said frames being defined as said last frame and receiving said delayed signal and generating a signal to activate said power return bus (e.g., col. 4, lines 26-31) and wherein the total count counter being incremented by each said pulse until said power return is activated (e.g., col. 8, lines 5-9).

Regarding claim 32, Beyers also discloses the ID counter represents the individual ID (e.g., col. 8, line 6).

Regarding claim 33, Beyers also discloses where the total count counter represents the total number connected together (e.g., col. 19, lines 22-24).

Regarding claim 34, Beyers discloses coupling a plurality of individual frames connected in series, a multi-channel bus coupled to each frame (e.g., col. 2, line 66 – col. 3, line 12), designating a last frame (e.g., col. 3, lines 10-12), designating one of the frames as a first frame (e.g., col. 4, lines 17-20) receiving a signal indicative of power being supplied to it and generating a delayed signal each subsequent frame receiving said delayed signal and generating a further delayed signal and each frame generating a pulse on said frame bus (e.g., col. 4, lines 15-17), generating a signal to activate said power return bus (e.g., col. 4, lines 26-31) and incrementing a register by each said pulse until said power return is activated (e.g., col. 8, lines 5-9).

Regarding claim 35, Beyers also discloses the ID counter represents the individual ID (e.g., col. 8, line 6).

Regarding claim 36, Beyers also discloses where the total count counter represents the total number connected together (e.g., col. 19, lines 22-24).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Cox (US 5901325) and Carbonneau (US 5966510) also disclose a frame system. Anderson (US 6633905) discloses a different embodiment of a frame system. Both Ono (US 2003/0194037) and Galloway (US 6493785) disclose enumeration for multi-frame systems.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clifford H Knoll whose telephone number is 703-305-8656. The examiner can normally be reached on M-F 0630-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

chk

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PRIMARY EXAMINER